**In the Specification**

At page 1, lines 8 – 15, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

The following patent documents are related to the present invention and are hereby incorporated by reference in their entirety; these U.S. Patent Applications are identified by their Serial Nos. as follows: 09/034,546, filed on March 3, 1998 and entitled "Thermally-induced Voltage Alteration (TIVA)", now U.S. Patent No. 6,078,183; and 09/586,505, entitled "Method and Apparatus for Analyzing Functional Failures In Integrated Circuits", now U.S. Patent No. 6,549,022~~(Docket No. SD6542S93805)~~ and 09/586,572, entitled "Data Processing Device Test Apparatus and Method Therefor", now U.S. Patent No. 6,546,513,~~(Docket No.184-P017US),~~ which have been concurrently filed herewith.

At page 2, lines 6 – 14, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

Many integrated circuit dies include circuits that are suspect defects, and these defects can recover or fail under particular operating conditions and at higher temperatures. For instance, circuit sites exhibiting temperature sensitive defects, such [[a]]as resistive connection, can recover when heated. Traditionally, isolation of IC defects has been attempted by operating the die in a manner that causes a failure to occur and by attempting to attribute the failure to a malfunctioning device in the IC. Such electrical testing, however, does not always work because many failures and malfunctions can result from a variety of different types of defects and defects at non-suspect circuitry locations.

At page 7, lines 20 – 23 and page 8, lines 1 – 5, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

One example of such operational failure results is when an electrical signal arrives at a destination too early or too late, resulting in an incorrect value of an output state of the IC. Circuit elements that can be involved with such failures include, for example, switching transistors or functional circuit blocks that switch between logic states at a rate that is slower than normal, and interconnections in the IC which have a resistance larger than an expected value. In general, anything within an IC that results in or contributes to a particular signal within the IC being advanced or delayed in propagation by one or more clock cycles, compared with the time at which the signal should appear, can result in an operational failure in the IC.

At page 10, lines 17 – 23 and page 11, lines 1 – 9, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

Operating an IC die under a failure condition can be accomplished in various manners. In some instances, the die is allowed to operate under normal operating conditions and is analyzed therefrom. In other instances, the die is operated under conditions that are selected to cause a failure condition. For example, the die can be operated under conditions that include selected clock speeds, temperatures, logic states, or other parameters that have been associated with a defect. In addition, the die can be operated using a selected test pattern that includes a pause in the signal to provide the die time to cool between cycles when being operated in a loop. Once a particular failure is identified to occur under a particular operating condition, that operating condition can be used to test the die under similar conditions to cause the failure to recur. In addition, the operating conditions can be selected so that the die fails at a selected failure rate, and variations in the failure rate that result in response to the application of heat can be used to analyze the die. For more information regarding the operation of an die die under failure conditions, reference may be made to the above-referenced U.S. Patent Application No. 09/034,546, now U.S Patent No. 6,078,183 entitled "Thermally-induced Voltage Alteration (TIVA)."

At page 14, lines 10 – 17, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

Also, a hardware latch, such as the latch shown in FIG. 5, or a software latch can be used to capture the logic state associated with the failure transition. One advantage of using a software latch is that the IC being tested is not placed under a load at the pin from which a signal is obtained. This is useful because loading the I/O pin can cause changes in the timing that can require a re-characterization of the IC being tested. For information regarding manners in which to test IC timing characteristics, reference may be made to U.S. Patent Application Serial No. ~~09/___,___,~~09/586,572 entitled "Data Processing Device Test Apparatus and Method Therefor", now U.S. Patent No. 6,546,513. ~~(Docket No.184-P017US).~~